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EXAMINER	
VELEZ, ROBERTO	

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2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,580	TANIOKA ET AL.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 6-7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagihara et al. (US Pat. 6,344,752).

Regarding claim 1, Hagihara et al. (shows Fig.1-2 and 10) an inspection probe [1] for inspecting electrical properties of a semiconductor device [W], comprising: a base member [2]; wiring layers [7] mounted on an outer surface of the base member [2]; probe pins [8] having tips [9A], the probe pins [8] electrically connected to and contacting the wiring layers [7], the probe pins [8] further protruding from the base member [2]; first metal layers [9B] provided to the tips [9A] of the probe pins [8]; and second metal layers [3] formed on the wiring layers [7], the second metal layers [3] being made of a material different from that of the probe pins [8] (any combination of nickel, nickel alloy, and nickel-cobalt alloy as suggested in Col. 5, Ln 15-18 and 58-60), wherein the first metal layers [9B] and the second metal layers [3] are physically separated from each other by the probe pins [8].

Regarding claim 4, Hagihara et al. discloses everything as claimed above in claim 1; in addition, Hagihara et al. shows (Figures 1-2) wherein the base member [2] has a plurality of the probe pins [8].

Regarding claim 6, Hagihara et al. discloses everything as claimed above in claim 1; in addition, Hagihara et al. discloses wherein the first metal layers [9B] and the second metal layers [3] are made of heterogeneous material (nickel and tungsten carbide, as disclosed in Col. 5, Ln 15-18 and 62-65).

Regarding claim 7, Hagihara et al. discloses everything as claimed above in claim 1; in addition, Hagihara et al. discloses wherein the first metal layers [9B] have hardness higher than that of the external terminal electrodes of the semiconductor device [W] (Col. 5, Ln 62-65).

Regarding claim 9, Hagihara et al. discloses everything as claimed above in claim 1; in addition, Hagihara et al. shows (Figures 2 and 10) wherein the probe pins [8] form an angle of 0 to 45 degrees with respect to a face on which the electrodes of the semiconductor device [W] are formed (As shown in figures 2 and 10, probe pins will be parallel to the electrodes of the semiconductor device. Therefore, probe pins 8 will form an angle of 0 degrees with respect to a face of the electrodes of the semiconductor device W.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara et al. (US Pat. 6,344,752).

Regarding claim 2, Hagihara et al. discloses everything as claimed above in claim 1.

Hagihara et al. fails to disclose wherein the first metal layers are made of a material having good contact properties selected depending on a material of external terminal electrodes of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first metal layers with a material having good contact properties selected depending on a material of external terminal electrodes of the semiconductor device. The ordinary artisan would have been motivated to modify Hagihara et al. in the manner set forth above for the purpose of using a material that will allow the first metal layers to obtain good measurements with high accuracy.

Regarding claim 3, Hagihara et al. discloses everything as claimed above in claim 1.

Hagihara et al. fails to disclose wherein the second metal layers have a volume resistivity less than that of the wiring layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second metal layers with a volume resistivity less than that of the wiring layers. The ordinary artisan would have been motivated to modify Hagihara et al. in the manner set forth above for the purpose of controlling the amount

of current or voltage being applied to the electrodes in order to avoid damaging the electrodes.

Regarding claim 5, Hagihara et al. discloses everything as claimed above in claim 1.

Hagihara et al. fails to disclose wherein the first metal layers and the second metal layers are made of homogeneous material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first metal layers and the second metal layers of homogeneous material. The ordinary artisan would have been motivated to modify Hagihara et al. in the manner set forth above for the purpose of saving cost on materials by avoiding the usage of different materials for the construction of the first metal layers and the second metal layers.

Regarding claim 8, Hagihara et al. discloses everything as claimed above in claim 1.

Hagihara et al. is silent about disclosing wherein a region for forming each first metal layer has a width wider than or equal to half of the width of the probe pins and a length longer than or equal to the sum of 1.0 time the size of the electrodes, the distance that the inspection probe is moved after the inspection probe coming in contact with the electrodes, the longitudinal positional tolerance of the probe pins, and the length determined based on the positional tolerance of the electrodes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make each first metal layer in a region that has a width wider

than or equal to half of the width of the probe pins and a length longer than or equal to the sum of 1.0 time the size of the electrodes, the distance that the inspection probe is moved after the inspection probe coming in contact with the electrodes, the longitudinal positional tolerance of the probe pins, and the length determined based on the positional tolerance of the electrodes. The ordinary artisan would have been motivated to modify Hagihara et al. in the manner set forth above for the purpose of maintaining a good contact alignment between probes and electrodes during testing in order to obtain high accuracy measurements.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara et al. (US Pat. 6,344,752) in view of Eldridge et al. (US Pat. 5,974,662).

Regarding claim 10, Hagihara et al. discloses everything as claimed above in claim 1; in addition, Hagihara et al. (shows Figures 2 and 10) a flexible, electrically connectable wiring substrate [11] placed between the base member [2] and an inspection substrate [T], for mounting the base member [2] thereon if the electrodes of the semiconductor device [W] are arranged at sides thereof, correspond to multiple pins [8], and must be connected to the inspection substrate [T].

Hagihara et al. fails to disclose wherein the first metal layers are made of a material having good contact properties selected depending on a material of external terminal electrodes of the semiconductor device. However, Eldridge et al. shows (Fig. 5) a flexible, electrically connectable wiring substrate [504] placed between the base member [506] and an inspection substrate [502] and a backup plate [530] mounted on the inspection substrate [502].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Eldridge et al. into the device of Hagihara et al. by having a flexible, electrically connectable wiring substrate placed between the base member and an inspection substrate and a backup plate mounted on the inspection substrate. The ordinary artisan would have been motivated to modify Hagihara et al. in the manner set forth above for the purpose of securing the inspection probe in order to obtain high accuracy measurements.

Allowable Subject Matter

7. Claims 11-20 are allowed.

8. The following is an examiner's statement of reasons for allowance: the prior art of record, taken alone or in combination, fails to disclose or render obvious, an inspection probe comprising a support substrate which is integrated with peripheral portions of the base member with an adhesive member placed there between and which is made of the same material as a material of the base member, said support substrate being mounted on the inspection substrate, wherein the backup plate has a protrusive portion at a center area thereof such that the probe pins form a predetermined angle with respect to the electrodes of the semiconductor device, in combination with all the limitations recited in claim 11.

Claims 12-20 depending from claim 11 are allowed for the same reason.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
10/19/2008

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829